UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARC TREMBLAY and WILLIAM JOY

Appeal No. 2005-1800
Application No. 09/204,479

HEARD: October 19, 2005

Before DIXON, GROSS, and BLANKENSHIP, ***Administrative Patent Judges***.

GROSS, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1, 3 through 17, 19 through 21, 23, and 24, which are all of the claims pending in this application.

Appellants' invention relates to instruction execution by a processor. In particular, a functional unit executes an instruction that operates on multiple registers in a register file, one of which is explicitly identified and another of which is implicitly identified based on the explicitly identified register. Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A processor comprising:

a register file; and

a functional unit, coupled to the register file, that executes an instruction that operates upon plural registers of said register file, including at least one register explicitly identified by an explicitly defined register specifier and at least one other register implicitly identified by the explicitly-defined register specifier.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Raghunathan et al. (Raghunathan)	4,300,195	Nov. 10, 1981
Baxter	5,826,096	Oct. 20, 1998

Andrew S. Tanenbaum, Structured Computer Organization, Prentice-Hall, Inc. (1976) pp. 75-87. (Tanenbaum)

Claims 1, 3 through 6, 8 through 17, 19 through 21, 23, and 24 stand rejected under 35 U.S.C. § 103 as being unpatentable over Baxter in view of Tanenbaum.

Claims 7 stands rejected under 35 U.S.C. § 103 as being unpatentable over Baxter in view of Tanenbaum and Raghunathan.

Reference is made to the Examiner's Answer (Paper No. 33, mailed March 8, 2004) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 32, filed January 20, 2004) and Reply Brief (Paper No. 34, filed May 13, 2004) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejections of claims 1, 3 through 17, 19 through 21, 23, and 24.

Independent claim 1 recites, in pertinent part, "an instruction that operates upon plural registers . . ., including at least one register explicitly identified by an explicitly defined register specifier and at least one other register implicitly identified by the explicitly-defined register specifier." Independent claim 20 recites method steps of explicitly defining one register that is operated upon during execution of an instruction and implicitly defining a second register that is also operated upon during execution of the instruction. Thus, one instruction operates upon at least two registers, one of which is explicitly identified, and the other of which is implicitly identified.

The examiner recognizes (Answer, page 3) that "Baxter does not show how register specifier . . . is developed." The examiner points to several sections of Tanenbaum to remedy this deficiency. Specifically, the examiner asserts (Answer, page 4)

that Tanenbaum discloses auto-indexing "wherein a one or a constant is automatically added to the previous address such that consecutively stored operands can be retrieved and operated upon by the op-code." The examiner continues, "If the operands of Baxter are consecutively stored, it would have been obvious to a person of ordinary skill in the art to use auto-indexing such that consecutively stored operands can be retrieved and acted upon by the op-codes." In the response to arguments section of the Answer, the examiner contends that "Tanenbaum is about auto-indexing of registers in register file which is exactly Appellants' invention."

Appellants argue (Brief, pages 6 and 7) that auto-indexing differs from the claimed implicit identification of a register. Specifically, appellants explain

> In auto-indexing, a register is incremented or decremented, *in preparation for use by a subsequent instruction*. Auto indexing is, therefore, inconsistent with the applicant's claimed invention, which requires implicitly identifying an additional register from an explicit register specifier of an instruction, where *the instruction operates on both the implicitly and explicitly identified registers*.

We agree with appellants. We find nothing in Tanenbaum to suggest two registers, one explicitly defined by an explicitly defined register specifier and a second implicitly identified by

the explicitly-defined register specifier, wherein one instruction operates upon both registers, as recited in claim 1. In the portion relied upon by the examiner (Section 3.3.6 of Tanenbaum) there is nothing to suggest that one instruction operates on both the explicitly defined register and the auto-indexed register. Thus, Tanenbaum fails to cure the deficiency of Baxter. Accordingly, we cannot sustain the obviousness rejection of claims 1 and 20, nor their dependents, claims 3 through 6, 8 through 17, 19, 21, 23, and 24. Further, since Raghunathan does not remedy the shortcomings of the primary combination, we cannot sustain the obviousness rejection of claim 7.

CONCLUSION

The decision of the examiner rejecting claims 1, 3 through 17, 19 through 21, 23, and 24 under 35 U.S.C. § 103 is reversed.

REVERSED

JOSEPH L. DIXON)
Administrative Patent Judge)
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ANITA PELLMAN GROSS) BOARD OF PATENT
Administrative Patent Judge) APPEALS
) AND
) INTERFERENCES
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HOWARD B. BLANKENSHIP)
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